IN THE CLAIMS

A listing of the pending claims is provided below.

1. (Previously Presented) A background memory manager (BMM) for managing a memory in a data processing system, the BMM comprising:

circuitry for transferring data structures to and from an outside device and to and from a memory;

a memory state map associated with the memory; and

a communication link to a processor;

characterized in that the BMM manages the memory, determining if each data structure fits into the memory, deciding exactly where to place each data structure in memory, performing all data transfers between the outside device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location.

2. (Previously Presented) The BMM of claim 1 wherein the BMM, in storing a given data structure, provides a data identifier for the given data structure on the link to the processor.

3. (Previously Presented) The BMM of claim 2 wherein the BMM, in making memory transactions, updates the memory state map to a new memory state, keeping track of regions occupied by valid data and regions not occupied by valid data.

4. (Previously Presented) The BMM of claim 2 wherein the BMM, in response to a signal on the processor link that the processor is finished with certain identified data in the memory, copies the identified data from the memory, if needed, to another device, and updates the memory state map to indicate a region of the identified data copied.

5. (Original) The BMM of claim 1 further comprising an interrupt handler allowing a remote data source to interrupt the BMM when data is available to be transferred to the memory.

6. (Previously Presented) The BMM of claim 1 wherein data handled by the BMM constitutes network data packets.

7. (Previously Presented) A data processing system, comprising:

a processor;

a memory coupled to the processor; and

a background memory manager (BMM) coupled to the memory and the processor, the background memory manager including circuitry for transferring data to and from an outside device and to and from the memory, and a memory state map associated with the memory;

characterized in that the BMM manages the memory, determining if each data structure fits into the memory, deciding exactly where to place the data structure in memory, performing all data transfers between the outside device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location.

8. (Previously Presented) The data processing system of claim 7 wherein the BMM, in storing a given data structure in the memory, provides a data identifier for the given data structure to the processor.

9. (Previously Presented) The data processing system of claim 8 wherein the BMM, in making memory transactions, updates the memory state map to a new memory state, keeping track of regions occupied by valid data and regions not occupied by valid data.

10. (Previously Presented) The data processing system of claim 8 wherein the BMM, in response to a signal from the processor that the processor is finished with certain

identified data in the memory, copies the identified data, if necessary, from the memory to another device, and updates the memory state map to indicate a region of the identified data copied.

11. (Original) The data processing system of claim 7 further comprising an interrupt handler allowing a remote data source to interrupt the BMM when data is available to be transferred to the memory.

12. (Previously Presented) The data processing system of claim 7 wherein data handled by the BMM constitutes network data packets.

13. (Previously Presented) A network packet router, comprising:

an input/output (I/0) device for receiving and sending packets on the network;

a processor;

a memory coupled to the processor; and

a background memory manager (BMM) coupled to the memory and the processor, the background memory manager including circuitry for transferring packets to and from the I/O device and to and from the memory, and a memory state map associated with the memory;

characterized in that the BMM manages the memory, determining if each data packet fits into the memory, deciding exactly where to place each data packet in memory, performing all data transfers between the outside device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location.

14. (Previously Presented) The data router of claim 13 wherein the BMM, in the process of storing a given packet into the memory, provides a data identifier for the given packet to the processor.

15. (Previously Presented) The data router of claim 14 wherein the BMM, in making memory transactions, updates the memory state map to a new memory state, keeping track of regions occupied by valid packets and regions not occupied by valid packets.

16. (Previously Presented) The data router of claim 14 wherein the BMM, in response to a signal that the processor is finished with a first packet in the memory, copies the first packet, if necessary, from the memory to the I/0 device, and updates the memory state map to indicate a region of the first packet copied.

17. (Original) The data router of claim 13 further comprising an interrupt handler allowing the I/0 device to interrupt the BMM when packets are available to be transferred to the memory.

18. (Previously Presented) A method for managing a memory in a data processing system having a processor, the method comprising:

(a) transferring data structures to and from an outside device and to and from the memory by circuitry in a background memory manager (BMM);

(b) determining by the BMM if each data structure from the outside device will fit into available space in the memory;

(c) deciding by the BMM exactly where in the memory to store each data structure; and

(d) updating a memory state map associated with the memory in the BMM each time a memory transaction is made.

19. (Previously Presented) The method of claim 18 wherein, in step (c), the BMM, in storing a given data structure into the memory, provides a data identifier for the given data structure on a link to the processor.

20. (Previously Presented) The method of claim 19 wherein the BMM, in step (b), in making memory transactions, updates the memory state map to a new memory state, keeping track of regions occupied by valid data and regions not occupied by valid data.

21. (Previously Presented) The method of claim 19 wherein, in step (a), the BMM, in response to a signal that the processor is finished with certain identified data in the memory, copies the identified data, if necessary, from the memory to another device, and updates the memory state map to indicate a region of the data copied.

22. (Original) The method of claim 18 further comprising a step for interrupting the BMM by the outside device when data is available to be transferred to the memory.

23. (Previously Presented) The method of claim 18 wherein data handled by the BMM constitutes network data packets.

24. (Original) The method of claim 23 wherein the network is the Internet.